REMARKS

This amendment responds to the office action mailed March 12, 2003. In the office action, the Examiner:

- rejected claims 1-5, 8-10 and 13-18 under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 5,668,599, Cheney; and
- rejected claims 6, 7, 11, 12, 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,668,599, Cheney, in view of U.S. Patent No. 5,276,851, Thacker.

After entry of this amendment, the pending claims are: claims 1-9, 13-14, and 16-22.

Summary of Claim Amendments

Claims 1 and 13 have been amended to indicate that cache memory, as opposed to main memory, is being analyzed to determine how the data store buffer sizes should be changed, and that the memory utilization data includes cache miss rate data. Claims 1 and 13 have also been amended to clarify that the scalable buffer is configured to the first buffer size and then to the second buffer size.

Claims 2, 6-9, and 14 have been amended for clarity.

Claims 10-12, 15, and 16-20 have been cancelled.

Claims 21 and 22 have been added.

The 35 U.S.C. § 102(b) Rejections

Claims 1-5, 8-10, and 13-18

The Examiner rejected claims 1-5, 8-9, 13-14, and 16-18 as being anticipated by Cheney. The Applicant respectfully traverses this rejection because these claims relate to cache memory and cache miss rates, while Cheney does not address cache memory or cache miss rates.

Claims 1 and 13, as amended, disclose a method or computer readable memory that monitors cache memory performance (cache miss rates) during the processing of a video data stream with a first buffer size and then a second buffer size. (Specification, pg. 5, lines 1-11.)

The buffer size is then adjusted based upon the cache performance results. (Specification, pg. 5, lines 11-17.) Cheney, however, relates to main memory utilization as opposed to cache memory utilization and, as revealed by a search of the Cheney text, does not mention the word "cache" at all.

Furthermore, although Cheney does change a buffer size, this change is based on the amount of data to be stored in the buffer, not on cache miss rates. Main memory use is vastly different from cache memory use. Multiple locations within main memory are frequently written to a single cache location. When the system requires data not already in the cache, the cache must evict existing data to make room for new data. This eviction process leads to misses when the system accesses the cache for data that has been evicted. There is no analogous eviction process for main memory use, so main memory does not have an associated miss rate. Cheney concerns main memory, and thus does not analyze cache performance or use cache miss rates as recited in claims 1 and 13 of the instant invention.

Since Cheney does not address cache memory or cache miss rates, Cheney does not teach or suggest the use of cache memory performance, and therefore does not anticipate claims 1 and 13, as amended. Claims 2-5, 8-9, 14, and 16-18, being dependent upon claims 1 and 13, are allowable for the same reasons claims 1 and 13 are allowable.

Claims 10 and 15 have been cancelled, making their rejections moot.

The 35 U.S.C. §103(a) Rejections

Claims 6, 7, 11, 12, 19, and 20

Claims 6, 7, 11, 12, 19, and 20 are rejected as unpatentable over Cheney in view of Thacker. The Applicant respectfully disagrees, however, because Thacker does not teach or suggest the use of a cache miss rate.

Claims 6, 7, 19, and 20 disclose creating cache utilization data defining data and instruction cache miss rates. These cache miss rates are to be a part of the memory utilization data analyzed to determine an efficient buffer size. (Specification, pg. 5, lines 10-17.) The instant invention thus teaches the use of cache miss rates to determine an efficient buffer size. Thacker, in contrary, does not teach the *use* of cache miss rates at all. What Thacker teaches is that by restricting frame buffer data to a small portion of the cache, the rate at which other types of data needed by the computer system are evicted from the cache by frame buffer data

is reduced. As a result, the overall cache miss rate of the system is improved (i.e., reduced), but Thacker does not use the cache miss rate to determine the portion of the cache to which frame buffer data should be restricted.

Since neither Thacker nor Cheney teach the use of cache miss rates to determine or adjust a buffer size, Thacker and Cheney combined do not teach or suggest every element of claims 6, 7, 19, and 20. Claims 6, 7, 19, and 20 are thus allowable.

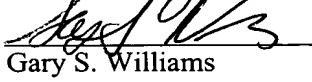
Claims 11 and 12 have been cancelled, making their rejections moot.

Conclusion

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 493-4935, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: May 2, 2003



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Gary S. Williams (Reg. No.)
PENNIE & EDMONDS LLP
3300 Hillview Avenue
Palo Alto, California 94304
(650) 493-4935